

# Low-Complexity Memoryless Linearizer for Analog-to-Digital Interfaces

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**Abstract**—This paper introduces a low-complexity memoryless linearizer for suppression of distortion in analog-to-digital interfaces. It is inspired by neural networks, but has a substantially lower complexity than the neural-network schemes that have appeared earlier in the literature in this context. The paper demonstrates that the proposed linearizer can outperform the conventional parallel memoryless Hammerstein linearizer even when the nonlinearities have been generated through a memoryless polynomial model. Further, a design procedure is proposed in which the linearizer parameters are obtained through matrix inversion. Thereby, the costly and time consuming iterative nonconvex optimization that is traditionally used when training neural networks is eliminated. Moreover, the design and evaluation incorporate a large set of multi-tone signals covering the first Nyquist band. Simulations show signal-to-noise-and-distortion ratio (SNDR) improvements of some 25 dB for multi-tone signals that correspond to the quadrature parts of OFDM signals with QPSK modulation.

## I. INTRODUCTION

Conversions between analog and digital signals are essential as the physical world is analog by nature whereas signal processing is primarily carried out in the digital domain. These transformations are implemented using analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), as well as other components required before/after the ADC/DAC, like filters, power amplifiers, and mixers. The overall converters are referred to as analog-to-digital and digital-to-analog interfaces (ADIs and DAIs), and this paper focuses on ADIs.

With the ever increasing demands for high-performance and low-cost signal processing and communication systems, there is a need to develop ADIs with higher performance in terms of data rates (related to bandwidths), effective resolution [effective number of bits (ENOB) determined by the signal-to-noise-and-distortion ratio (SNDR)<sup>1</sup>], and low implementation cost (small chip area and low energy consumption). This project focuses on the SNDR which in analog circuits is degraded by nonlinearities. The SNDR can consequently be increased by using linearization techniques which are required to reach a large SNDR. However, linearization can also be utilized for low/medium SNDRs as it enables the use of one- or few-bits ADCs, below the targeted SNDR which is

subsequently achieved through digital processing. Thereby the energy consumption of the ADCs can be reduced substantially as their energy consumption is very high for large SNDRs, especially when the data rate is also high [1]. For example, the 14-bit converter AD9699 from Analog Devices [2] has a power consumption of about 2 W at a data rate of 3 GS/s. It is particularly important to reduce the ADC power in applications requiring many ADCs like in massive-MIMO communication systems [3]. However, to reach the targeted SNDR, keeping the overall energy consumption low, it is then vital to develop energy efficient digital linearizers.

In a practical ADI, nonlinearities in the analog circuitry introduce distortion which degrades the SNDR and ENOB. If the distortion is frequency-independent, one can use memoryless polynomial modeling and linearization, which is in focus in this paper. This model is typically sufficient for narrow to medium bandwidths and resolutions. To reach higher resolutions over wider frequency bands, one may need to incorporate memory (subfilters) in the modeling and linearization.

### A. Contribution of the Paper and Relation to Previous Work

In the conventional memoryless linearizer, the distortion is suppressed by using a special case of a parallel Hammerstein system (Fig. 1 in Section II) [4]. This system incorporates  $K$  branches, realizing the terms  $c_k v^k(n)$ ,  $k = 1, 2, \dots, K$ , where  $v(n)$  is the distorted signal. The implementation cost of such a scheme emanates from both the  $K$  multiplications between  $c_k$  and  $v^k(n)$  and the generation of the  $K - 1$  nonlinearity terms  $v^k(n)$ .

In this paper, we introduce a memoryless linearizer (Fig. 2 in Section II) where the nonlinearity terms  $v^p(n)$  are replaced by the simpler nonlinearities  $|v(n)|$  or  $\max\{0, v(n)\}$  (rectified linear unit) as they can be implemented in hardware with low complexity. In addition, bias values are added before the nonlinearities. The proposed linearizer is inspired by neural networks, but the neural-network schemes that have appeared earlier in the literature in this context have a very high implementation complexity (several hundreds of multiplications in [5] and several thousands of multiplications in [6]). The implementation complexity of the proposed linearizer is substantially lower and it will be demonstrated that it can outperform the conventional parallel Hammerstein linearizer even when the nonlinearities have been generated through a memoryless polynomial model.

<sup>1</sup>ENOB = (SNDR - 1.76)/6.02.

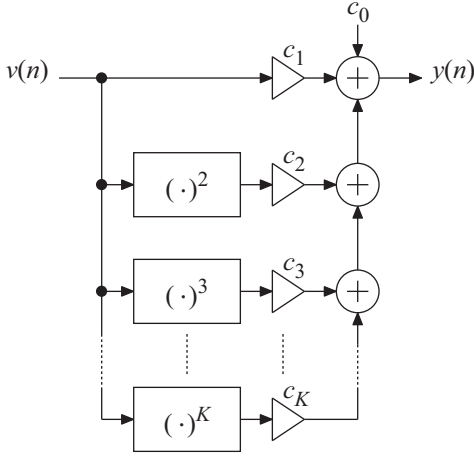


Fig. 1. Hammerstein linearizer.

Further, a design procedure is proposed in which the parameters (corresponding to the multipliers  $c_k$  above) are obtained through matrix inversion. Thereby, one can eliminate the costly and time consuming iterative nonconvex optimization that is traditionally used when training neural networks [5], [6]. Moreover, the design and evaluation incorporate a large set of multi-tone signals covering the first Nyquist band. In the previous works [5], [6], the evaluation has only included a few single-tone signals. Our simulations show SNDR improvements up to some 25 dB for multi-tone signals that correspond to the quadrature parts of OFDM signals with QPSK modulation.

Finally, it is noted that neural networks have also been considered for predistortion of power amplifiers (PAs) required in DAIs, see for example [7], [8] and references therein. However, those techniques are not directly applicable for ADI linearization which is in focus here. A major difference is that, for ADIs, the nonlinearities can be undersampled and still suppressed provided the signal is Nyquist sampled [9]. In DAIs, the predistorted signal must be oversampled to enable distortion cancellation in the analog domain.

## B. Outline

Following this introduction, the signal model, Hammerstein linearizer, and proposed linearizer are presented in Section II. Section III presents the proposed design procedure, whereas simulations, results, and comparisons are provided in Section IV. Finally, Section V concludes the paper.

## II. SIGNAL MODEL, HAMMERSTEIN LINEARIZER, AND PROPOSED LINEARIZER

Let the desired discrete-time signal be  $x(n) = x_a(nT)$  which corresponds to an analog signal  $x_a(t)$  sampled uniformly with a sampling frequency of  $1/T$ . In addition, the signal contains noise but this is not included in the mathematical expressions below for the sake of simplicity. It is further assumed that the distorted signal, say  $v(n)$ , can be modeled as a memoryless polynomial according to

$$v(n) = a_0 + a_1 x(n) + \sum_{p=2}^P a_p x^p(n), \quad (1)$$

where  $a_0$  is a constant,  $a_1$  is a linear-distortion constant, and  $a_p, p = 2, 3, \dots, P$ , are  $P - 1$  nonlinear-distortion constants. In the conventional parallel Hammerstein linearizer, depicted in Fig. 1, the linearized signal, say  $y(n)$ , is formed as

$$y(n) = c_0 + c_1 v(n) + \sum_{k=2}^K c_k v^k(n). \quad (2)$$

In an implementation, this scheme requires  $2K - 1$  multiplications and  $K$  two-input additions per sample ( $K$  multiplications for generating  $c_k v^k(n)$ , and  $K - 1$  multiplications for generating  $v^k(n)$ ).

Before proceeding, it is noted that, to be able to model the signal as in (1) in a practical system, the parameters  $a_k$  need to be estimated. There are several methods available for this purpose [4]. However, the focus of this paper is to linearize the distorted signal, and the model in (1) is then used for generating sets of test and evaluation signals. It is stressed though that the proposed linearizer (to be described below) does not assume that the distorted signal is in the form of the polynomial in (1).

## A. Proposed Linearizer

Given a distorted signal  $v(n)$ , the output signal  $y(n)$  in the proposed linearizer, depicted in Fig. 2, is formed as

$$y(n) = c_0 + c_1 v(n) + \sum_{m=1}^N w_m u_m(n) \quad (3)$$

where

$$u_m(n) = f_m(v(n) + b_m), \quad (4)$$

with  $f_m$  being nonlinear operations. Here,  $f_m(v) = |v|$  or  $f_m(v) = \max\{0, v\}$  due to their low hardware implementation complexity, as noted in [7] where  $f_m(v) = \max\{0, v\}$  was utilized in a predistorter. Further, the bias values  $b_m, m = 1, 2, \dots, N$ , are assumed to be uniformly distributed between  $-b_{\max}$  and  $b_{\max}$ , where the value of  $b_{\max}$  is optimized as outlined in Section III. That is,  $b_m$  are given by

$$b_m = -b_{\max} + \frac{2(m-1)b_{\max}}{N-1}. \quad (5)$$

In an implementation, the proposed scheme requires only  $N + 1$  multiplications per sample with  $N$  nonlinear branches, and  $2N + 1$  two-input additions due to the additional  $N$  bias additions. An additional advantage of the proposed linearizer is that it does not require any quantizations before the multiplications. In the Hammerstein linearizer, on the other hand, quantizations are required at the outputs of the nonlinearities (i.e., before the multiplications) to avoid very long and costly internal wordlengths. This introduces quantization errors (quantization noise) which are scaled by the coefficients  $c_k$ . Therefore, those coefficients have to be kept small to avoid a large noise amplification which would degrade the output SNDR. Alternatively, longer internal wordlengths are needed but it also increases the implementation cost. This problem is circumvented by using the proposed scheme where all quantizations take place after all multiplications. Hence, there is no noise amplification from the quantizations to the output in the proposed scheme.

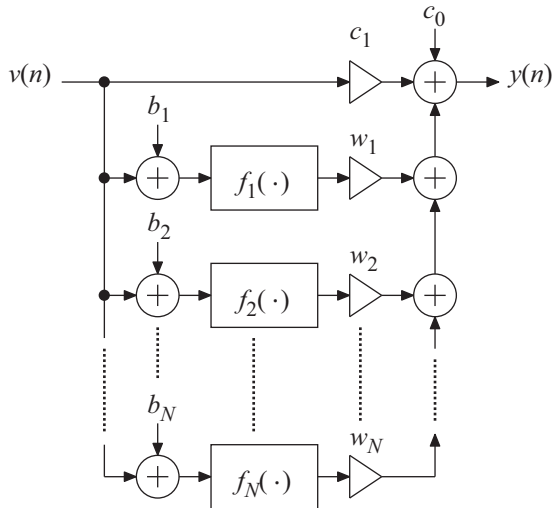


Fig. 2. Proposed linearizer.

### III. PROPOSED DESIGN

The design of the proposed linearizer amounts to determining the parameters  $c_0$ ,  $c_1$ ,  $w_m$ , and  $b_m$  so that the output signal  $y(n)$  approximates the desired signal  $x(n)$  as well as possible in some sense which is here assumed to be the least-squares sense. For this purpose, we propose the following design procedure where it is assumed that the signal is normalized so that its modulus is bounded by one.

- 1) Generate a set of  $R$  reference signals  $x_r(n)$  and the corresponding distorted test signals  $v_r(n)$ ,  $r = 1, 2, \dots, R$ , using a signal model as in (1) or measured data.
- 2) Generate a set of  $Q$  uniformly distributed values of  $b_{\max} \in [b_l, b_u]$ . We have experimentally observed that  $b_l = 0.5$  and  $b_u = 1.5$  are appropriate values when the signal is within the range  $-1$  to  $1$ .
- 3) For each value of  $b_{\max}$ , compute  $b_m$  according to (5). Then, minimize the cost function  $E$  as given by

$$E = \sum_{r=1}^R \sum_{n=1}^L (y_r(n) - x_r(n))^2, \quad (6)$$

where  $L$  is the data length. All coefficients  $c_0$ ,  $c_1$ , and  $w_m$ ,  $m = 1, 2, \dots, N$ , in (3) are computed via a matrix inversion, including  $L_2$ -regularization to avoid large parameter values. To be precise, let  $\mathbf{w}$  be a  $(N+2) \times 1$  column vector containing all coefficients  $w_m$ ,  $m = 1, 2, \dots, N$ ,  $c_1$ , and  $c_0$ , and  $\mathbf{A}_r$  be an  $L \times (N+2)$  matrix where the columns  $l$ ,  $l = 1, 2, \dots, N+2$ , contain the  $L$  samples  $u_{r,m}(n)$ ,  $m = 1, 2, \dots, N$ ,  $L$  input samples  $v_r(n)$ , and  $L$  ones (for the constant  $c_0$ ). Then, minimizing  $E$  in (6) in the least-squares sense gives the solution

$$\mathbf{w} = \mathbf{A}^{-1} \mathbf{b}, \quad (7)$$

where

$$\mathbf{A} = \lambda \mathbf{I} + \sum_{r=1}^R \mathbf{A}_r^T \mathbf{A}_r, \quad \mathbf{b} = \sum_{r=1}^R \mathbf{A}_r^T \mathbf{b}_r, \quad (8)$$

with  $\mathbf{A}_r^T$  being the transpose of  $\mathbf{A}_r$  and  $\mathbf{b}_r$  being an  $L \times 1$  column vector containing the  $L$  samples  $x_r(n) - v_r(n)$ . It is noted here that  $x_r(n) - v_r(n)$  is used in  $\mathbf{b}_r$  instead of  $x_r(n)$ , in order to compute a small value of  $c_1$ . That is, we are replacing  $c_1 v(n)$  in (3) with  $v(n) + \Delta c_1 v(n)$  and then compute the value of  $\Delta c_1$ . In this way, all parameters to be computed in the least squares design are then small (zero in the ideal case with no distortion). Further,  $\lambda \mathbf{I}$  is a diagonal matrix with small diagonal entries  $\lambda$  for the  $L_2$ -regularization. It is noted that each corrected output  $y_r(n)$  (when the signals are interpreted as column vectors) can be computed as

$$y_r(n) = v_r(n) + \mathbf{A}_r \mathbf{w}. \quad (9)$$

- 4) Select the best of the  $Q$  solutions above.
- 5) Evaluate the linearizer over a large set of signals, say  $M$  signals, where  $M \gg R$ .

### IV. SIMULATIONS, RESULTS, AND COMPARISONS

We assume a distorted signal  $v(n)$  as in (1) with the parameters<sup>2</sup>  $a_0 = 0$ ,  $a_1 = 1$ ,  $a_p = (-1)^p \times 0.15/p$ ,  $p = 2, 3, \dots, P$ , and  $P = 10$ . The signal  $x(n)$  is selected as

$$x(n) = \frac{0.9}{31} \times \sum_{k=1}^{31} A_k \sin(\omega_k n + \alpha_k), \quad (10)$$

where

$$\omega_k = \frac{2\pi k}{64} + \Delta\omega. \quad (11)$$

This signal corresponds to the quadrature part (imaginary part) of an OFDM signal with 31 active carriers out of 64 carriers and frequency offset represented by  $\Delta\omega$ . Further, we assume QPSK modulation which means that  $A_k = 1$  for all  $k$  whereas  $\alpha_k$  are randomly generated from the four possible angles  $\pi/4$ ,  $-\pi/4$ ,  $3\pi/4$ , and  $-3\pi/4$ . The scaling constant 0.9 is included to ensure that the magnitude of the distorted signal is less than one.

In the design, we use only one such signal (thus  $R = 1$  in Section III), with all  $\alpha_k$  being zero but with a random frequency offset. In the evaluation, we use  $M = 500$  signals with randomly generated frequency offsets assuming uniform distribution between  $-\pi/64$  and  $\pi/64$ . All signals are of length  $L = 2^{13}$  and quantized to 12 bits. Further, we have considered both  $f_m(v) = |v|$  and  $f_m(v) = \max\{0, v\}$  for the nonlinear operations. The results below are for  $f_m(v) = |v|$  but the other option gave the same results. For the  $L_2$ -regularization, we have used  $\lambda = 0.02$ .

Figure 3 plots the spectrum before and after linearization for one of the signals. Figure 4 plots the SNDR using both the proposed linearizer and the Hammerstein linearizer, which has been designed in the same way as the proposed linearizer but without the bias values. When comparing the implementation complexities for the same SNDR, one should however not use the number of branches but rather the number of multiplications and additions required, of which the multiplications are the most expensive ones to implement. Recall from Section II

<sup>2</sup>We have also considered the case with  $a_0 \approx 0$  and  $a_1 \approx 1$  and obtained the same results.

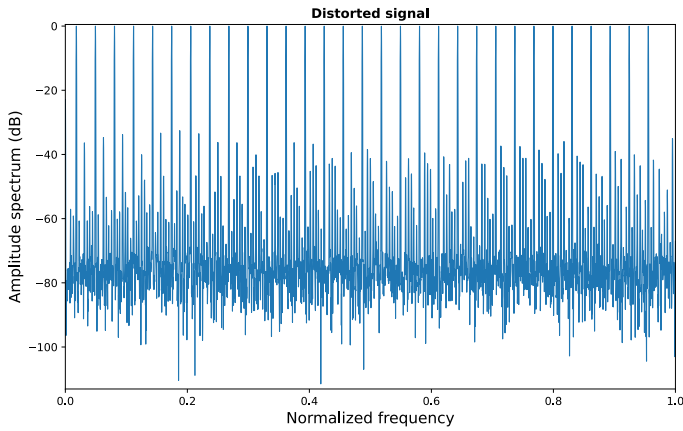


Fig. 3. Spectrum before and after linearization for one of the signals using the proposed linearizer with  $N = 16$  nonlinear branches.

that the Hammerstein linearizer requires  $2K - 1$  multiplications for  $K - 1$  nonlinear branches whereas the proposed linearizer requires only  $N + 1$  multiplications for  $N$  nonlinear branches. To take this into account, Fig. 5 plots the SNDR versus the multiplication complexity.

As seen in Fig. 5, the proposed linearizer outperforms the Hammerstein linearizer when the number of multiplications exceeds four. Furthermore, it is noted that for the signal considered in this example, quantized to 12 bits, the SNR is approximately 58 dB when there is no distortion. As seen in Fig. 4, the SNDR approaches this value for the proposed linearizer when the number of nonlinear branches increases. With about 20 nonlinear branches, the SNDR is close to 58 dB. For the Hammerstein linearizer, the SNDR saturates at a lower level. This is due to the  $L_2$ -regularization which is needed to keep the multiplier values  $c_k$  small to avoid large quantization noise amplification, as discussed in Section II-A. With  $\lambda = 0.02$ , used in this example, all multiplier values are below some  $1/2$  in magnitude which means that at most a few additional bits are needed internally in the Hammerstein linearizer. As also discussed in Section II-A, such quantization amplification does not exist in the proposed linearizer but the modulus of  $w_m$  and  $c_1$  are below some  $1/2$  here as well.

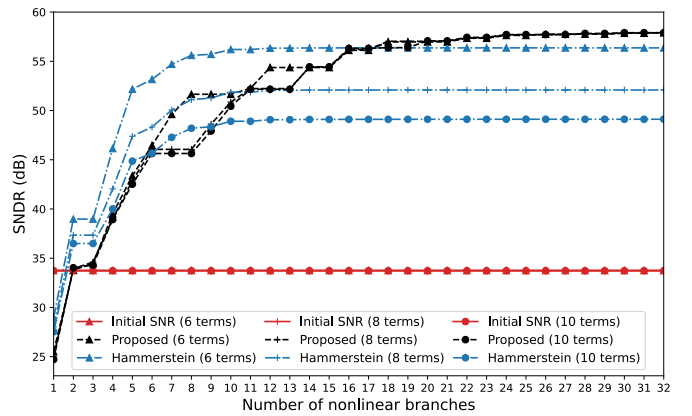


Fig. 4. SNDR versus number of nonlinearity branches.

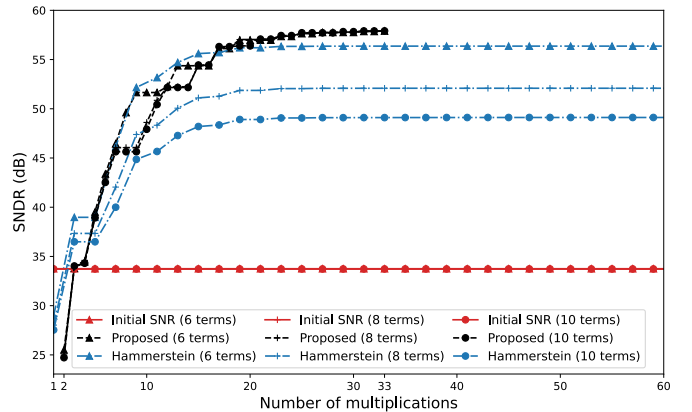


Fig. 5. SNDR versus number of multiplications.

## V. CONCLUSION

This paper introduced a low-complexity memoryless linearizer for suppression of distortion in analog-to-digital interfaces. It is inspired by neural networks, but has a substantially lower complexity than traditional neural-network schemes (as seen in Fig. 5). Simulations demonstrated SNDR improvements of some 25 dB for multi-tone signals that correspond to the quadrature parts of OFDM signals with QPSK modulation. Thereby, the SNDR approached the SNR of such multi-tone signals quantized to 12 bits. It was also demonstrated that the proposed linearizer can outperform the conventional parallel memoryless Hammerstein linearizer, both in terms of low implementation complexity for the same SNDR, and in terms of feasible SNDR improvements.

Furthermore, a design procedure was proposed in which all linearizer parameters are obtained through matrix inversion, thereby avoiding the costly and time-consuming iterative nonconvex optimization that is traditionally used when training neural networks. Ongoing work studies the extension to low-complexity memory linearizers addressing frequency-dependent nonlinearities (memory polynomials).

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